Competence Center for
Advanced Network Technologies and Systems

GMD FOKUS

The ATM-Sat Demonstrator

Related Activities within the ATM-Sat Project

Presentation to Industry Representatives and Interested Scientists

http://www.fokus.gmd.de
http://www.fokus.gmd.de/cats

Falco Krepel / Hartmut Brandt
ATM Sat Workshop

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  - mobile terminal
  - satellite
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- Demonstrator vs. Target System
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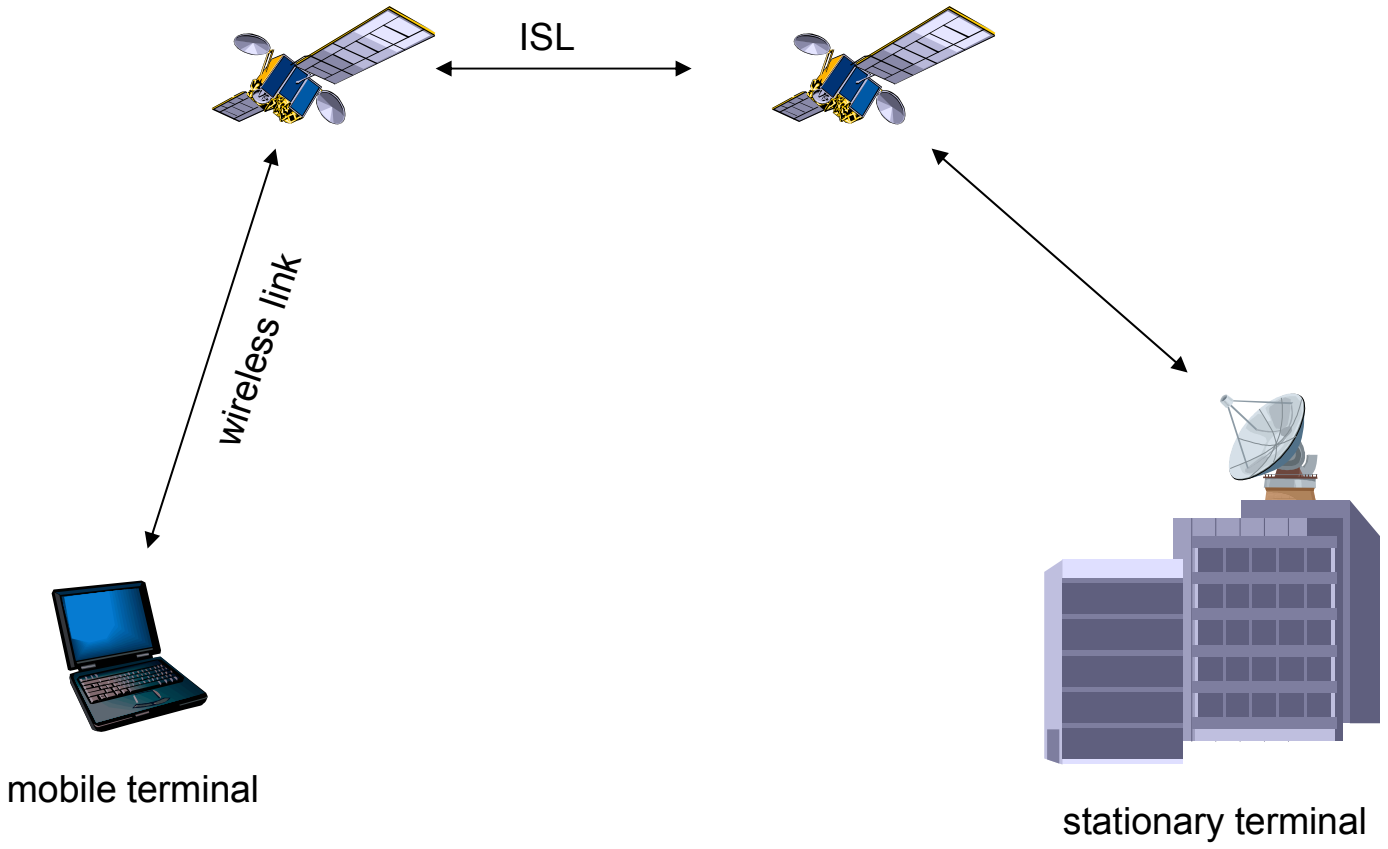
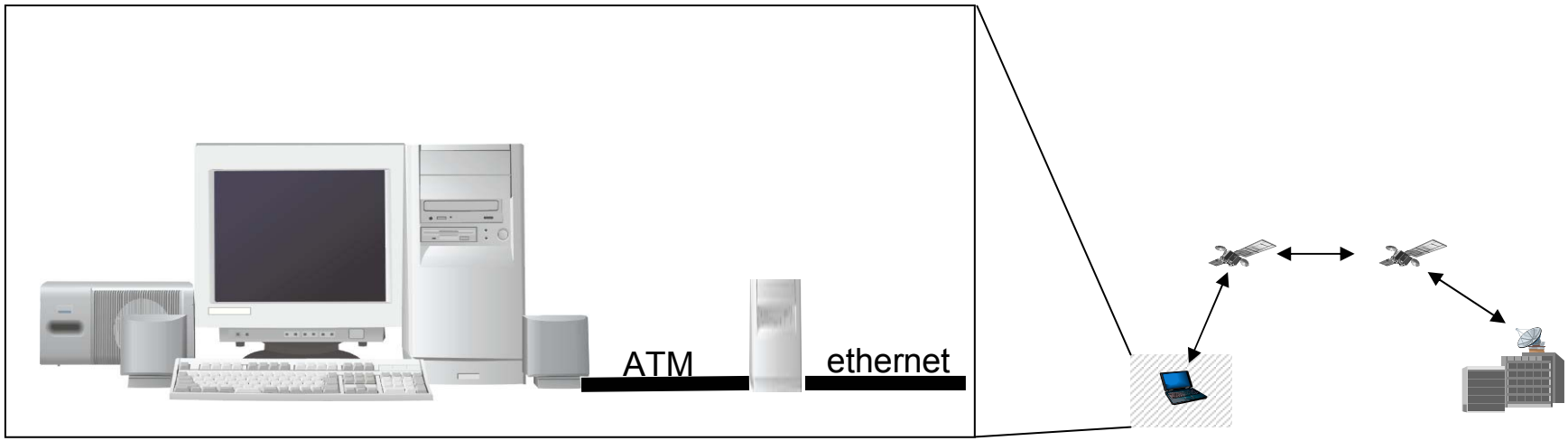
Target Environment (example)



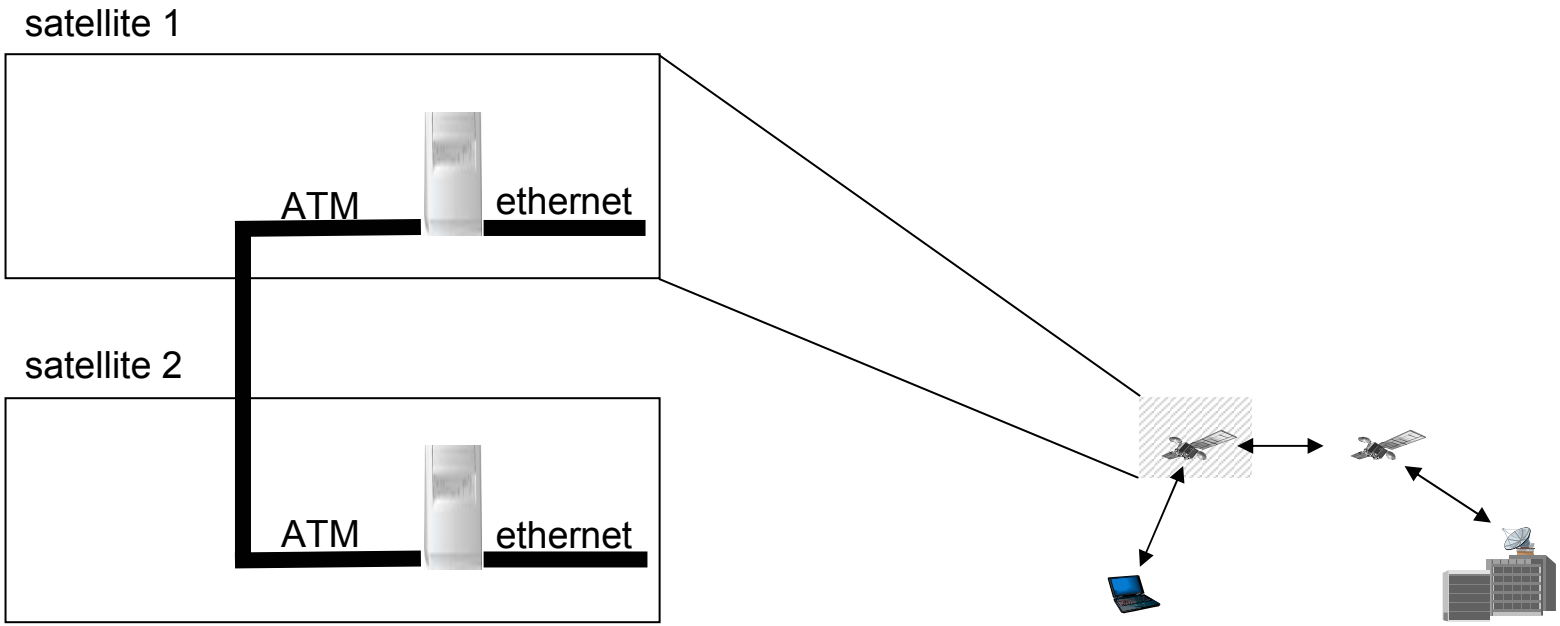
Mobile Terminal

- splitted in two computing hosts (workhost, MAC-layer)
- connected via ATM
- looks like one system for applications



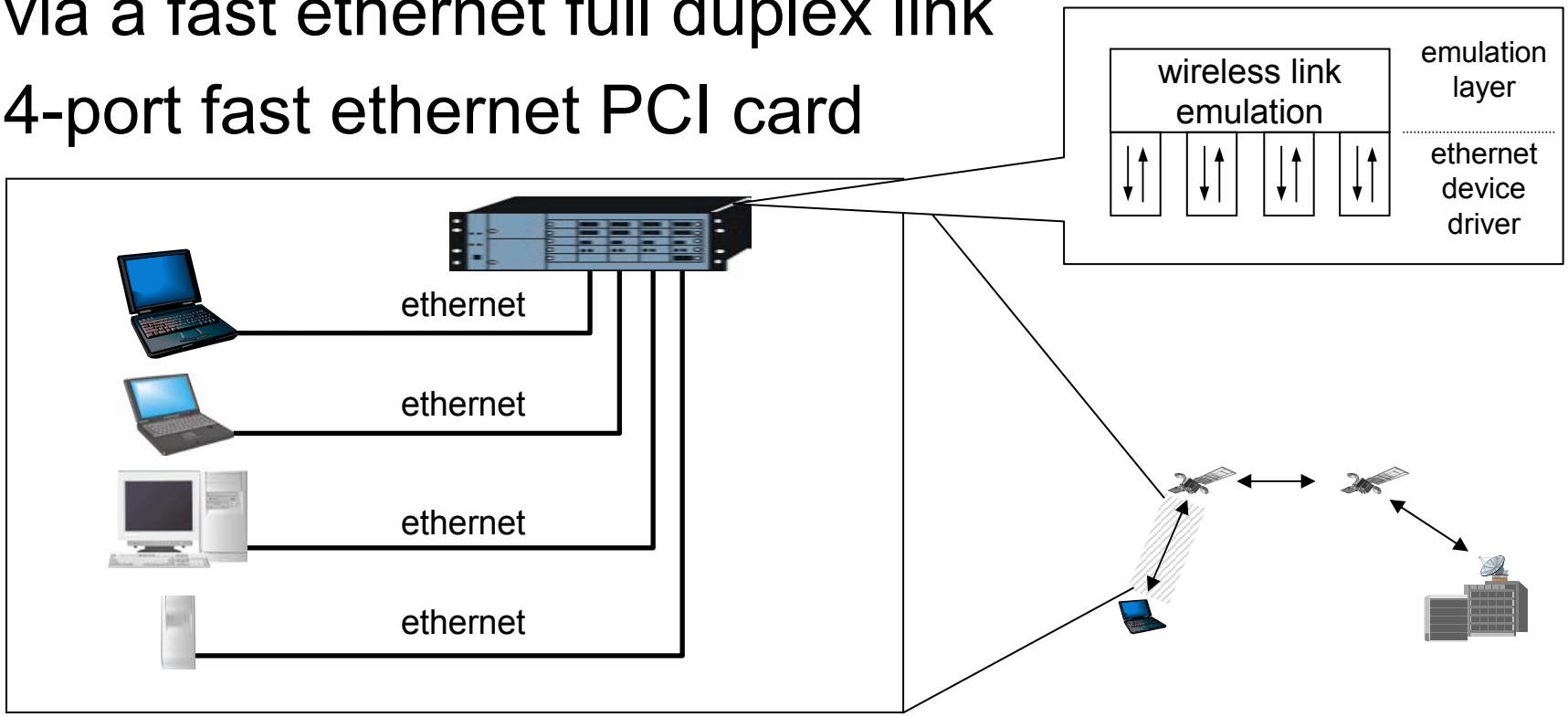
Satellite

- one computing host (MAC-layer)
- connected via ATM (ISL)

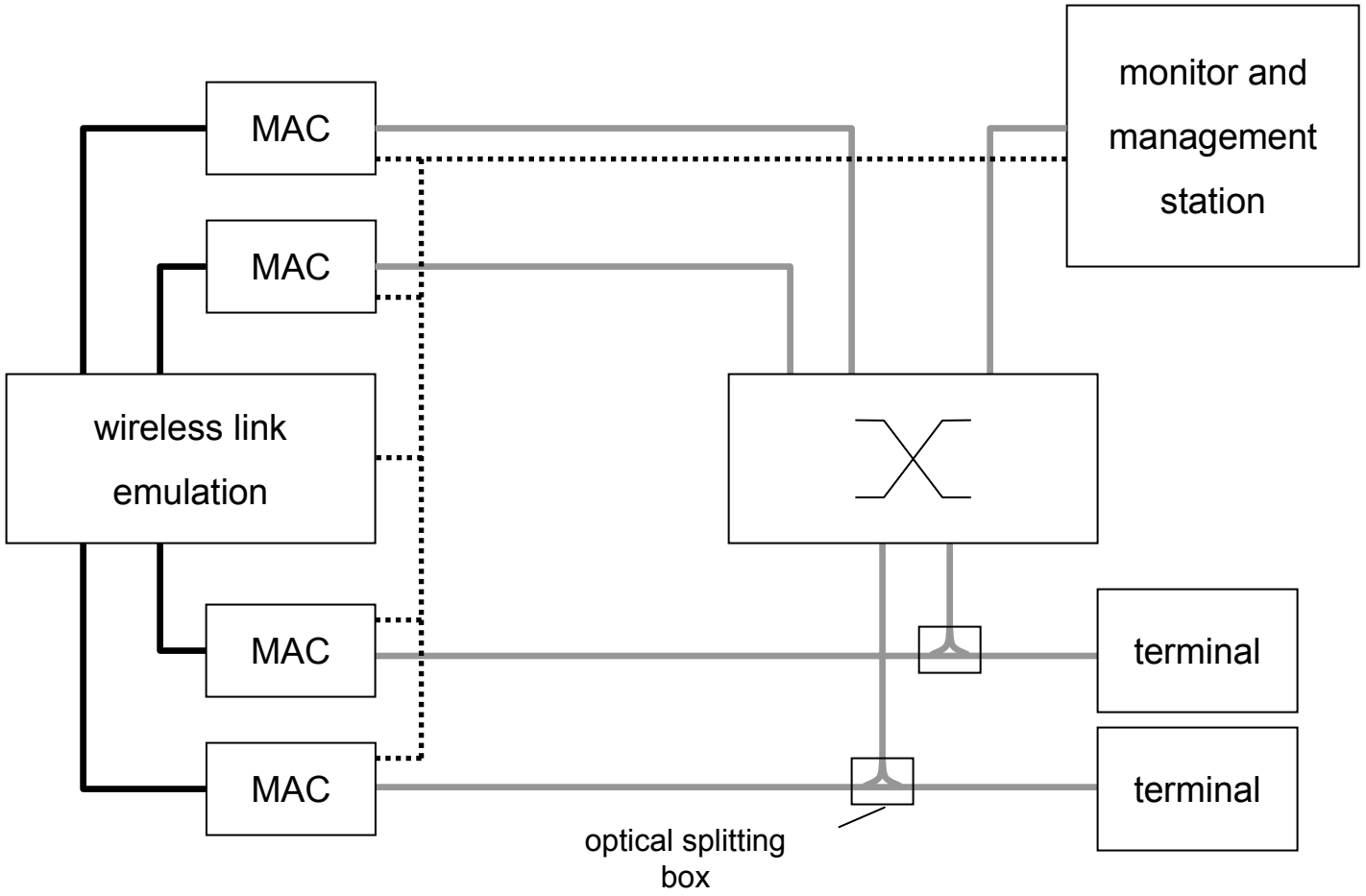


Wireless Link

- realised as software emulation
- each MAC-layer is connected via a fast ethernet full duplex link
- 4-port fast ethernet PCI card

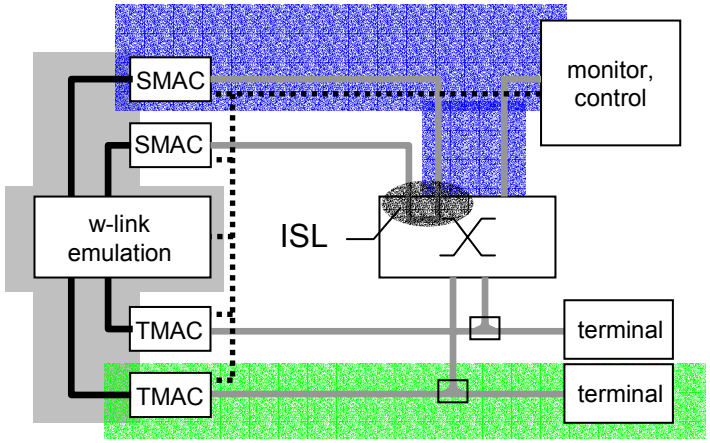


Demonstrator

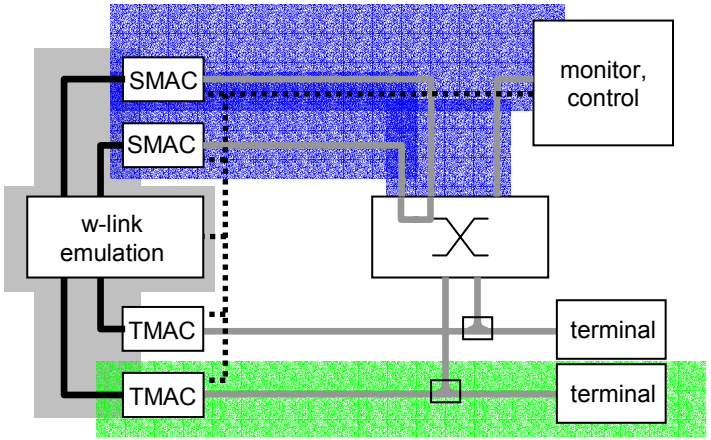


Demonstrator vs. Target System

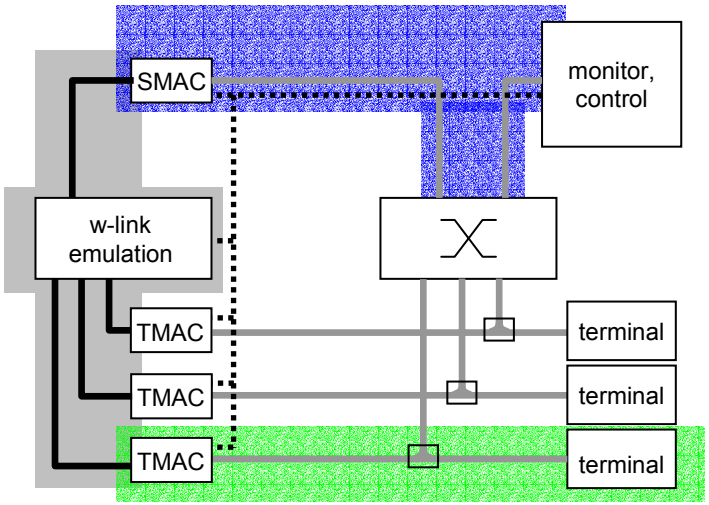
2 terminals resides in different footprints of two satellites



2 terminals resides in different spotbeams of one satellite

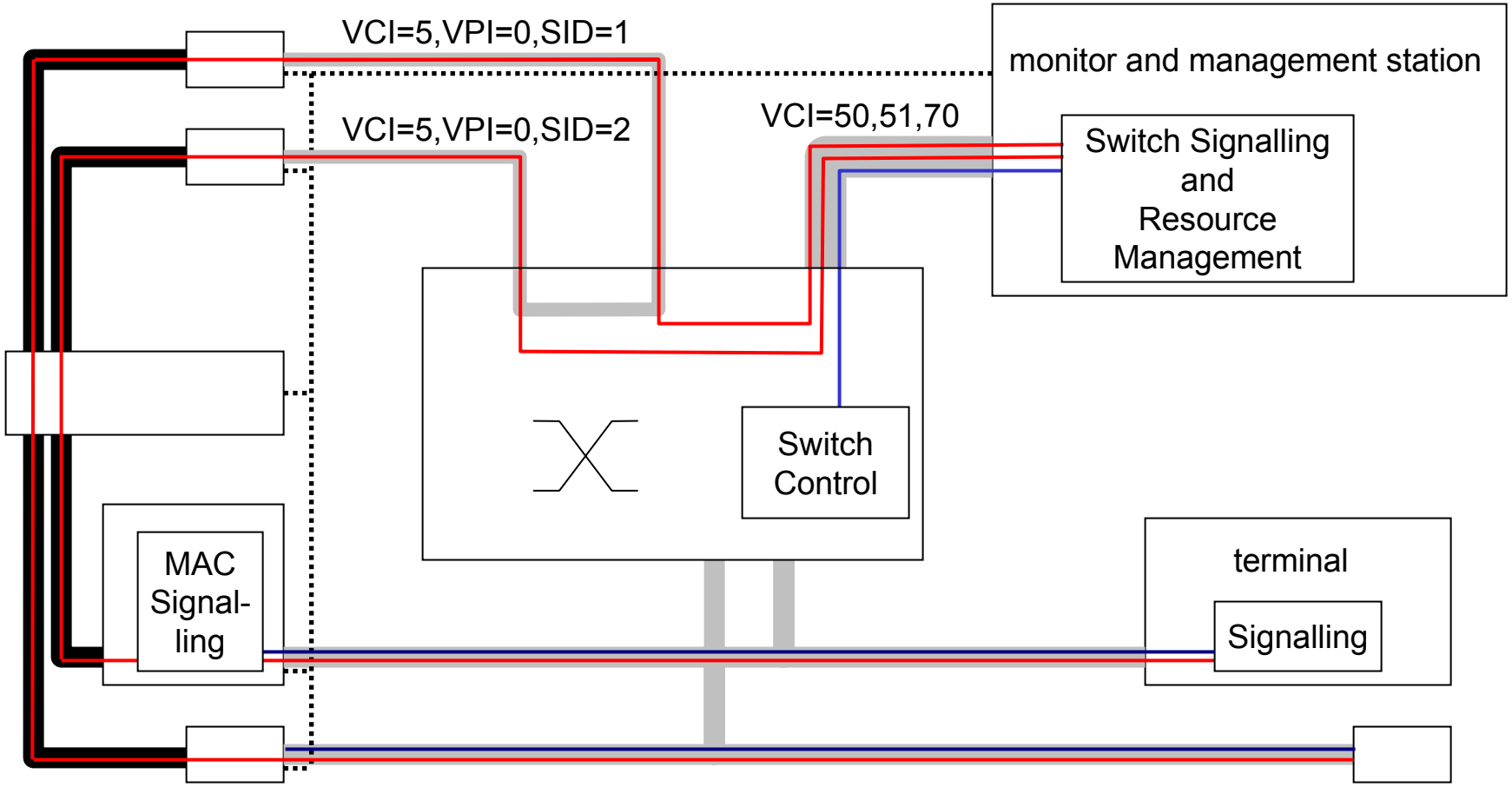


3 terminals resides in one spotbeam



satellite | *wireless link* | *user terminal*

Signalling



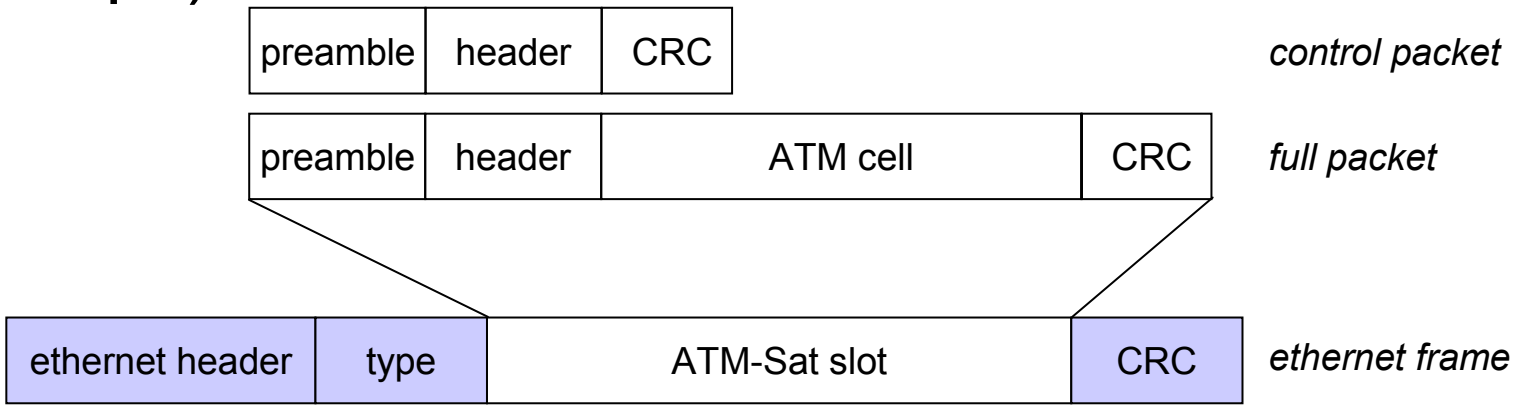
Switch control (SNMP/CLIP)

Signalling

UNI/MAC interface

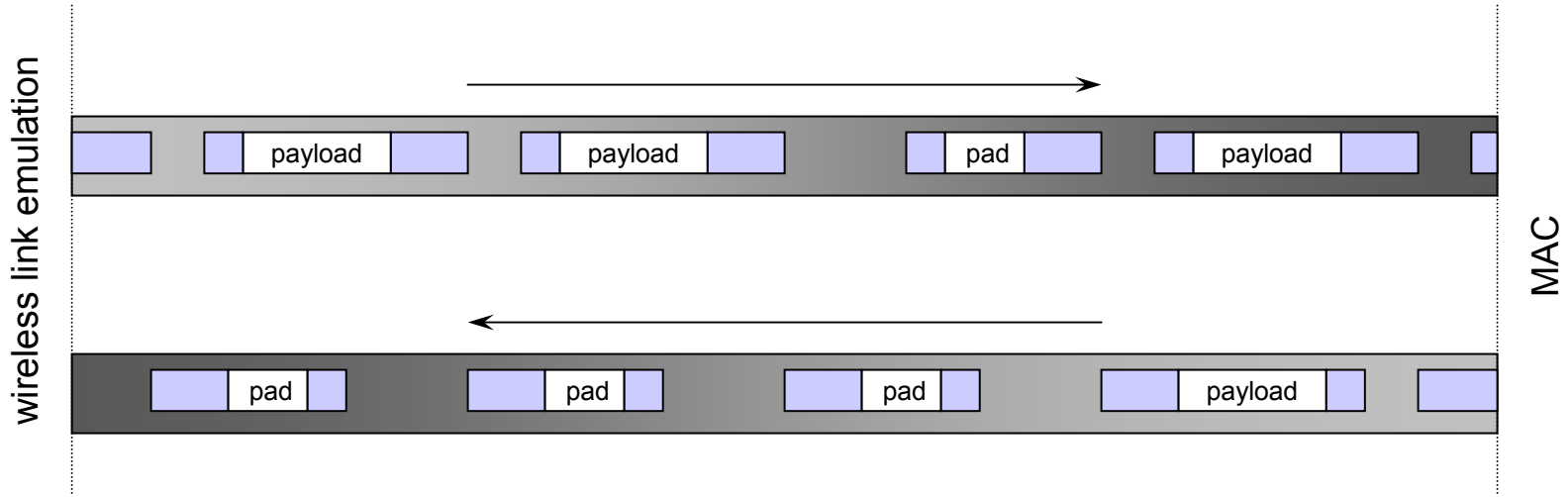
Wireless Link Emulation via Ethernet (basics)

- 100 Mbit/s full-duplex ethernet point-to-point links
- collision free
- each slot encapsulated in one ethernet frame
- special sync information within each packet or NTP is used for clock synchronisation (accuracy 10-100 µs)



Wireless Link Emulation via Ethernet (link)

- one frame is always send after a specified time depending on uplink/downlink frame structure



System Load Check

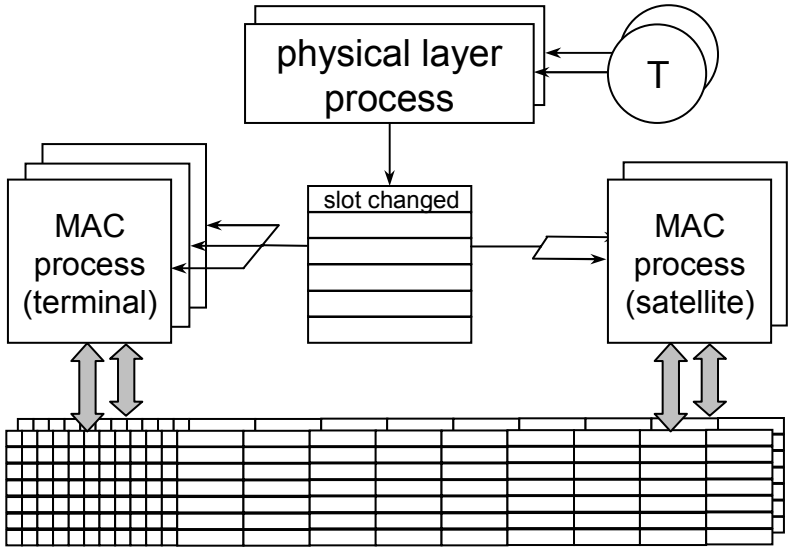
	ethernet frame size	demonstrator slot size	ethernet frame duration	demonstrator slot duration
control packet	72 byte	17 byte	5,76 µs	43,52 µs
full packet	96 byte	70 byte	7,68 µs	179,2 µs

	theoretical	*real system*
frame could be send every	control packet → **6,72 µs**	demonstrator → **53,12 µs**
	full packet → **8,46 µs**	demonstrator → **188,16 µs**
used bandwith		maximum at MAC → **8,3 Mbit/s**
		maximum at w-link → **33,2 Mbit/s**

no timing problems, no heavy load

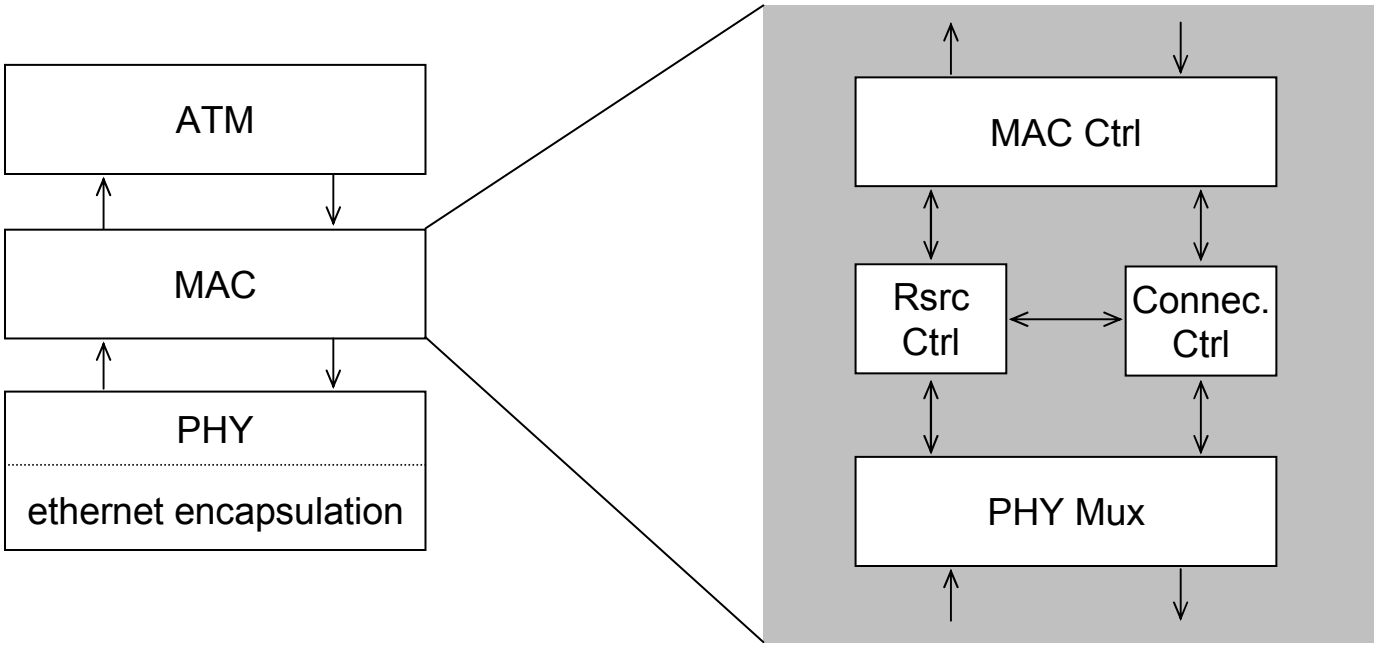
Software Simulation of MAC Layer

- completely modeled in software
- a complete MAC layer is one process
- two processes for the physical layer (uplink/downlink)
- each process work on a shared data structure
- synchronised through broadcasted signal



Protocol Stack Overview

- MAC layer same as in simulation
- physical layer looks like a real physical layer
- PHY encapsulates the slots in ethernet frames



Future Work

- setup the demonstrator with all components
- measure the synchronisation accuracy
- implement the framework for software simulation
- port the framework to the demonstrator environment
- verify the system